National Semiconductor

PRELIMINARY
December 1994

NM27LV040/NM27LV040B 4,194,304-Bit (512k x 8) Low Voltage CMOS EPROM

General Description

The NM27LV040/NM27LV040B is a high performance Low Voltage Electrically Programmable Read Only Memory. It is manufactured using National's latest 0.8μ CMOS AMG™ EPROM technology. This low voltage technology allows the low power part to operate at speeds as fast as 100 ns over industrial temperatures (−40°C to +85°C). This product is ideal for using in handheld battery powered systems to maximize the battery usage.

The NM27LV040B has a voltage tolerance range of 2.7V–3.6V, ideal for unregulated power supply. The NM27LV040 is optimized for 3.3V and has a voltage tolerance range of ±0.3V.

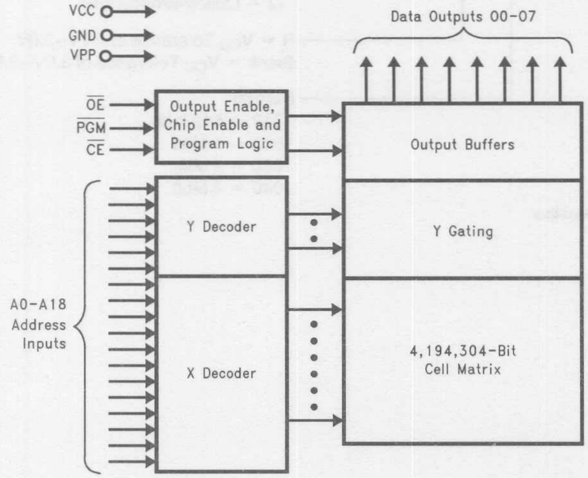
Since both low power and small outline packages are critical to portable applications, National provides windowed LCC packages for prototyping and software development, PLCC and TSOP for production.

This product is ideal for power sensitive, space sensitive applications which demand high performance such as digital cellular phones.

Features

- 3.0V to 3.6V operation
- 2.7V to 3.6V operation (unregulated)
- 100 ns access time
- Low Current Operation
  - — 12 mA Typical I_{CC} Active @ 5 MHz
  - — 50 μA Typical I_{CC} Standby @ 5 MHz
- Ultra low power operation (Typical)
  - — 40 mW Active Power @ 3.3V
  - — 165 μW Standby Power @ 3.3V
- Surface mount package options
  - — 32-pin TSOP
  - — 32-pin PLCC

Block Diagram



TL/D/12328-1

Pin Names

A0–A18	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O0–O7	Outputs
$\overline{PGM}$	Program
XX	Don't Care

TRI-STATE® is a registered trademark of National Semiconductor Corporation.
AMG is a trademark of WSI, Incorporated.

Ordering Information

Commercial Temp. Range (0°C to +70°C)
V_{CC} = 3.3V ±0.3V

Parameter/Order Number	Access Time (ns)
NM27LV040 Q, V, T 90	90
NM27LV040 Q, V, T 120	120
NM27LV040 Q, V, T 150	150
NM27LV040 Q, V, T 200	200

Industrial Temp. Range (−40°C to +85°C)
V_{CC} = 3.3V ±0.3V

Parameter/Order Number	Access Time (ns)
NM27LV040 QE, VE, TE 100	100
NM27LV040 QE, VE, TE 120	120
NM27LV040 QE, VE, TE 150	150
NM27LV040 QE, VE, TE 200	200

Commercial Temp. Range (0°C to +70°C)
V_{CC} = 2.7V −3.6V

Parameter/Order Number	Access Time (ns)
NM27LV040B Q, V, T 100	100
NM27LV040B Q, V, T 120	120
NM27LV040B Q, V, T 150	150
NM27LV040B Q, V, T 200	200

*All versions are guaranteed to function at slower speeds.

Industrial Temp Range (−40°C to +85°C)
V_{CC} = 2.7V −3.6V

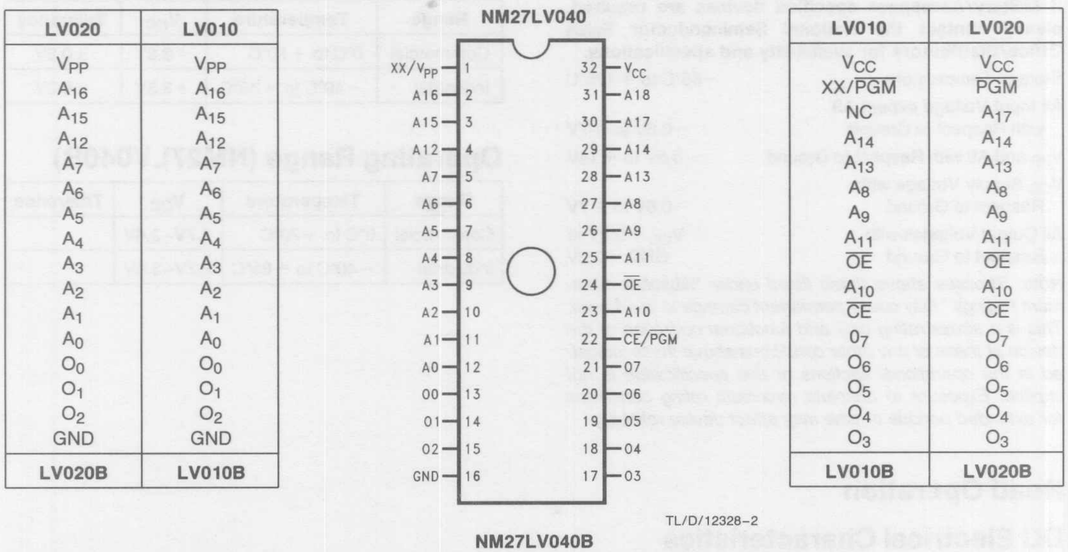
Parameter/Order Number	Access Time (ns)
NM27LV040B QE, VE, TE 100	100
NM27LV040B QE, VE, TE 120	120
NM27LV040B QE, VE, TE 150	150
NM27LV040B QE, VE, TE 200	200

NM 27 LV 040 B V E 100

- NM — National Memories
- 27 — EPROM
- LV — Low Voltage
- 100 — Speed
  100 ns
- E — Operating Temp
  Blank = Commercial Temp.
  E = Industrial Temp.
- V — Packaging
  V = PLCC
  T = TSOP
  Q = Quartz-window DIP
- B — B = V_{CC} Tolerance of 2.7V−3.6V
  Blank = V_{CC} Tolerance of 3.0V−3.6V
- 040 — Density
  512 = 512 k-bit
  010 = 1 Mbit
  020 = 2 Mbit
  040 = 4 Mbit

Note: When ordering Advance CMOS product please specify standard flow.

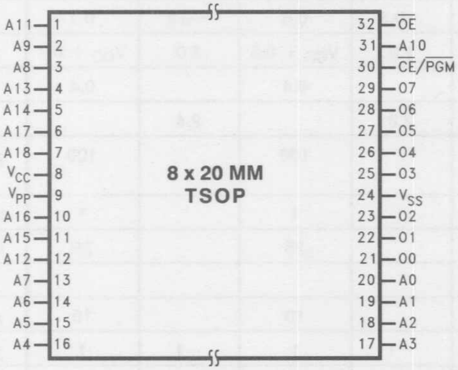
Connection Diagrams



TL/D/12328-2

Note: Compatible EPROM pin configurations are shown in the blocks adjacent to the NM27L040/NM27LV040B pin.

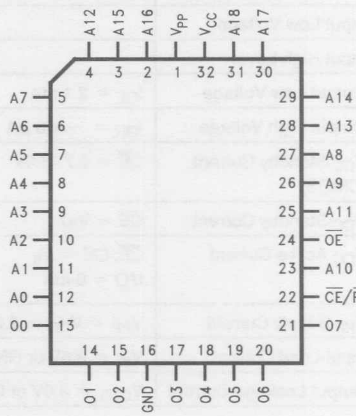
TSOP Pin Configuration



TL/D/12328-3

Top View

PLCC Pin Configuration



TL/D/12328-4

Top View

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +125°C
All Input Voltage expect A9 with Respect to Ground	−0.6V to +7V
V_{PP} and A9 with Respect to Ground	−0.6V to +14V
V_{CC} Supply Votlage with Respect to Ground	−0.6V to +7V
All Output Voltages with Respect to Ground	V_{CC} +0.5V to GND −0.3V

Note: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.*

Operating Range (NM27LV040)

Range	Temperature	V_{CC}	Tolerance
Commercial	0°C to +70°C	+3.3V	±0.3V
Industrial	−40°C to +85°C	+3.3V	±0.3V

Operating Range (NM27LV040B)

Range	Temperature	V_{CC}	Tolerance
Commercial	0°C to +70°C	2.7V–3.6V	
Industrial	−40°C to +85°C	2.7V–3.6V	

Read Operation

DC Electrical Characteristics

Symbol	Parameter	Test Conditions		V_{PP} = 2.7V–3.6V		V_{PP} = 3.3V ±10%		Units
				Min	Max	Min	Max	
V_{IL}	Input Low Voltage			−0.3	0.6	−0.3	0.7	V
V_{IH}	Input High Level			2.0	V_{CC} + 0.5	2.0	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			0.4		0.4	V
V_{OH}	Output High Voltage	I_{OH} = −400 µA		2.2		2.4		V
I_{SB1} (Note 3)	V_{CC} Standby Current (CMOS)	$\overline{CE}$ = 2.7–3.6V			100		100	µA
I_{SB2}	V_{CC} Standby Current	$\overline{CE}$ = V_{IH}			1		1	mA
I_{CC} (Note 1)	V_{CC} Active Current	$\overline{CE}$, OE = V_{IL} I/O = 0 mA	f = 5 MHz		25		25	mA
I_{PP}	V_{PP} Supply Current	V_{PP} = V_{CC} = 3.6V			10		10	µA
I_{LI}	Input Load Current	V_{IN} = 3.6V or GND		−1	1	−1	1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 3.6V or GND		−1	10	−1	10	µA

AC Electrical Characteristics (Over operating range with V_{PP} = V_{CC})

Symbol	Parameter	100		120		150		200		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		100		120		150		200	ns
t_{CE}	CE to Output Delay		100		120		150		200	ns
t_{OE}	OE to Output Delay		40		40		50		50	ns
t_{DF} (Note 2)	Output Disable to Output Float		30		30		30		55	ns
t_{OH}	Output Hold from Addresses, CE or OE, whichever Occurred First	0		0		0		0		ns

Note 1: The supply current is the sum of I_{CC} and I_{PP}. The maximum current value is with Outputs O_0 to O_7 unloaded.

Note 2: This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.

Note 3: CMOS inputs: V_{IL} = GND ±0.3V, V_{IH} = V_{CC} ±0.3V.

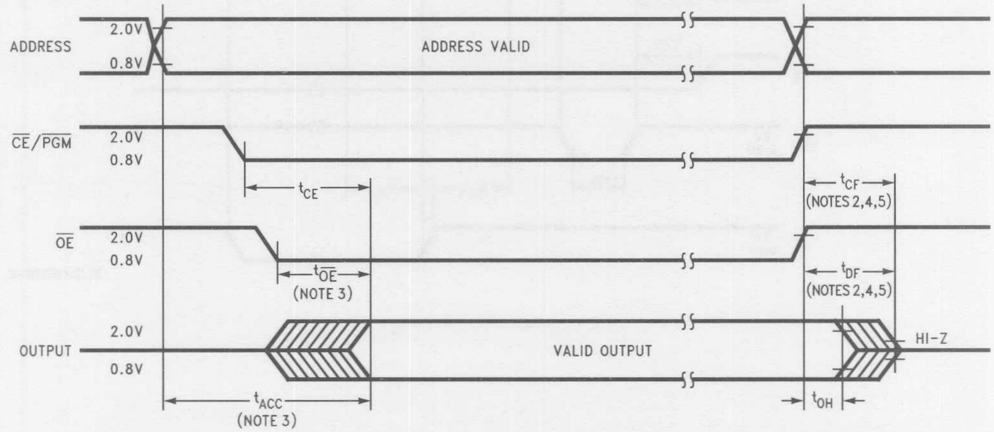
Capacitance $T_a = +25°C$, f = 1 MHz (Note 2)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	$V_{IN} = 0V$	9	15	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	12	15	pF

AC Test Conditions

Output Load	1 TTL Gate and $C_L = 100$ pF (Note 8)
Input Rise and Fall Times	≤ 5 ns
Input Pulse Levels	0.45V to 2.4V
Timing Measurement Reference Level (Note 10)	
Inputs	0.8V and 2V
Outputs	0.8V and 2V

AC Waveforms (Notes 6, 7, and 9)



TL/D/12328–5

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 4: The t_{DF} and t_{CF} compare level is determined as follows:
High to TRI-STATE®, the measured V_{OH1} (DC) −0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) +0.10V.

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 MF ceramic capacitor be used on every device between V_{CC} and GND.

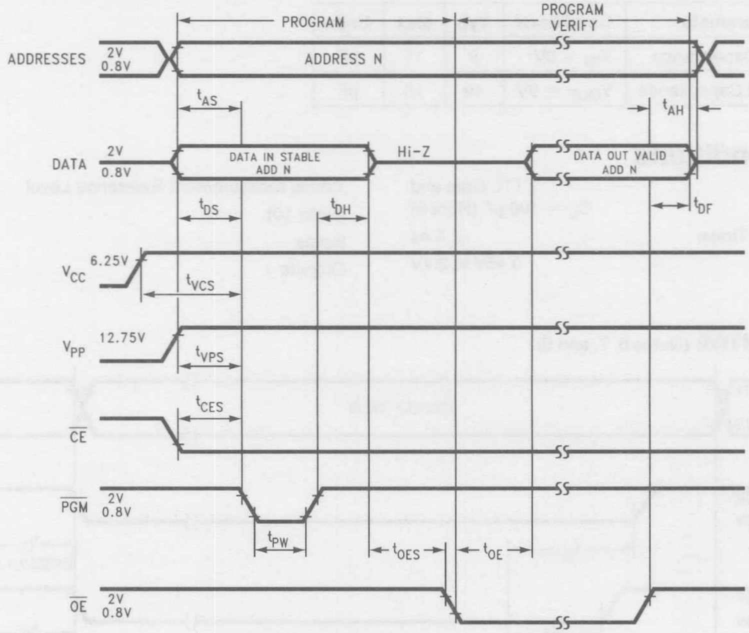
Note 7: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

Note 8: 1 TTL Gate: $I_{OL} = 1.6$ mA, $I_{OH} = -400$ μA.
C_L: 100 pF includes fixture capacitance.

Note 9: V_{PP} may be connected to V_{CC} except during programming.

Note 10: Inputs and outputs can undershoot to −2.0V for 20 ns Max.

Programming Waveforms (Note 3)



TL/D/12328-6

Programming Characteristics (Notes 1, 2, 3, 4, and 5)

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{AS}	Address Setup Time		1			μs
T_{OES}	$\overline{OE}$ Setup Time		1			μs
T_{DS}	Data Setup Time		1			μs
T_{VPS}	V_{PP} Setup Time		1			μs
T_{VCS}	V_{CC} Setup Time		1			μs
T_{AH}	Address Hold Time		0			μs
T_{DH}	Data Hold Time		1			μs
T_{DF}	Output Enable to Output Float Delay	$\overline{CE}/\overline{PGM} = X$	0		60	μs
T_{PW}	Program Pulse Width		95	100	105	μs
T_{OE}	Data Valid from $\overline{OE}$	$\overline{CE}/\overline{PGM} = X$			100	ns
I_{PP}	V_{PP} Supply Current during Programming Pulse	$\overline{CE}/\overline{PGM} = V_{IL}$			30	mA
I_{CC}	V_{CC} Supply Current				50	mA
T_A	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		6.0	6.25	6.5	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13.0	V
T_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage		−0.1	0.0	0.45	V
V_{IH}	Input High Voltage		2.4	4.0		V
t_{IN}	Input Timing Reference Voltage		0.8		2.0	V
t_{OUT}	Output Timing Reference Voltage		0.8		2.0	V

Note 1: National's standard product warranty applies only to devices programmed to specifications described herein.

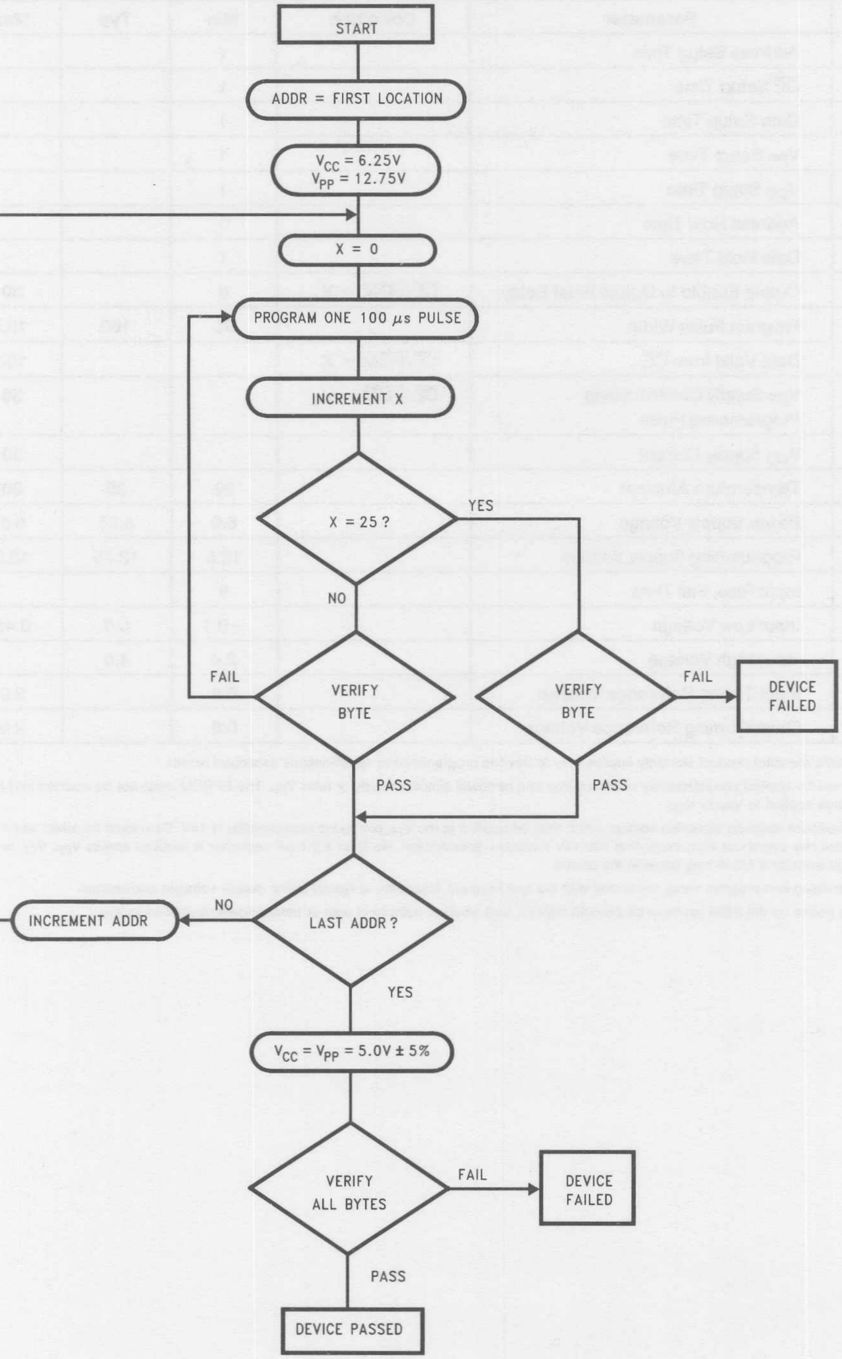
Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board wth voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. As least a 0.1 μF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested with the fast Program Algorithm, at typical power supply voltages and timings.

Note 5: During power up the PGM pin must be brought high ($\leq V_{IH}$) whether coincident with or before power is applied to V_{PP}.

Fast Programming Algorithm Flow Chart



TL/D/12328-7

Functional Description

Device Operation

The six modes of operation of the EPROM are listed in Table I. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are V_{CC} and V_{PP}. The V_{PP} power supply must be at 12.75V during the three programming modes and must be at 3.3V in the other three modes.

Read Mode

The EPROM has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}/\overline{PGM}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

Standby Mode

The EPROM has a standby mode which reduces the active power dissipation by over 99%, from 40 mW to 0.17 mW. The EPROM is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}/\overline{PGM}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output Disable

The EPROM is placed in output disable by applying a TTL high signal to the $\overline{OE}$ input. When in output disable all circuitry is enabled, except the outputs are in a high impedance state (TRI-STATE).

Output OR-Tying

Because the EPROM is usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}/\overline{PGM}$ be decoded and used as the primary device selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all selected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on pin 1 (V_{PP}) will damage the EPROM.

Initially, and after each erasure, all bits of the EPROM are in the "1's" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The EPROM is in the programming mode when the V_{PP} power supply is at 12.75V and $\overline{OE}$ is at V_{IH}. It is required that at least a 0.1 μF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, an active low, TTL program pulse is applied to the $\overline{PGM}$ input. A program pulse must be applied at each address location to be programmed. The EPROM is programmed with the Fast Programming Algorithm shown in *Figure 1*. Each Address is programmed with a series of 100 μs pulses until it verifies good, up to a maximum of 25 pulses. Most memory cells will program with a single 100 μs pulse.

The EPROM must not be programmed with a DC signal applied to the $\overline{PGM}$ input.

Programming multiple EPROM in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the parallel EPROM may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{PGM}$ input programs the paralleled EPROM.

Note: Some programmer manufacturers, due to equipment limitation, may offer interactive program Algodthm (shown in *Figure 2*).

Functional Description (Continued)

Program Inhibit

Programming multiple EPROMs in parallel with different data is also easily accomplished. Except for $\overline{CE}/\overline{PGM}$, all like inputs (including $\overline{OE}$) of the parallel EPROMs may be common. A TTL low level program pulse applied to an EPROM's $\overline{CE}/\overline{PGM}$ input with V_{PP} at 12.75V will program that EPROM. A TTL high level $\overline{CE}/\overline{PGM}$ input inhibits the other EPROMs from being programmed.

PROGRAM VERIFY

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 12.75V. V_{PP} must be at V_{CC} except during programming and program verify.

AFTER PROGRAMMING

Opaque labels should be placed over the EPROM window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

MANUFACTURER'S IDENTIFICATION CODE

The EPROM has a manufacturer's identification code to aid in programming. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

The Manufacturer's Identification code, shown in Table II, specifically identifies the manufacture and device type. The code for NM27LV040/NM27LV040B is "8F08", where "8F" designates that it is made by National Semiconductor, and "08" designates a 4 Megabit (512k x 8) part.

The code is accessed by applying 12V $\pm$0.5V to address pin A9. Addresses A1–A8, A10–A16, and all control pins are held at V_{IL}. Address pin A0 is held at V_{IL} for the manufacturer's code, and held at V_{IH} for the device code. The code is read on the eight data pins, O_0–O_7. Proper code access is only guaranteed at 25°C $\pm$5°C.

Erasure Characteristics

The erasure characteristics of the device are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range.

The recommended erasure procedure for the EPROM is exposure to short wave ultraviolet light which has a wavelength of 2537Å. The integrated dose (i.e., UV intensity x exposure time) for erasure should be minimum of 45W-sec/cm^2.

The EPROM should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure. Table III shows the minimum EPROM erasure time for various light intensities.

An erasure system should be calibrated periodically. The distance from lamp to device should be maintained at one inch. The erasure time increases as the square of the distance from the lamp. (If distance is doubled the erasure time increases by factor of 4.) Lamps lose intensity as they age. When a lamp is changed, the distance has changed, or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

System Consideration

The Power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent of the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

Mode Selection

The modes of operation of the NM27LV040 are listed in the following table. Single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and A_9 for device signature.

Pins / Mode	CE/PGM	OE	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	X (Note 1)	5.0V	D_{OUT}
Output Disable	X	V_{IH}	X	5.0V	High Z
Standby	V_{IH}	X	X	5.0V	High Z
Programming	V_{IL}	V_{IH}	12.75V	6.25V	D_{IN}
Program Verify	V_{IL}	V_{IL}	12.75V	6.25V	D_{OUT}
Program Inhibit	V_{IH}	X	12.75V	6.25V	High Z

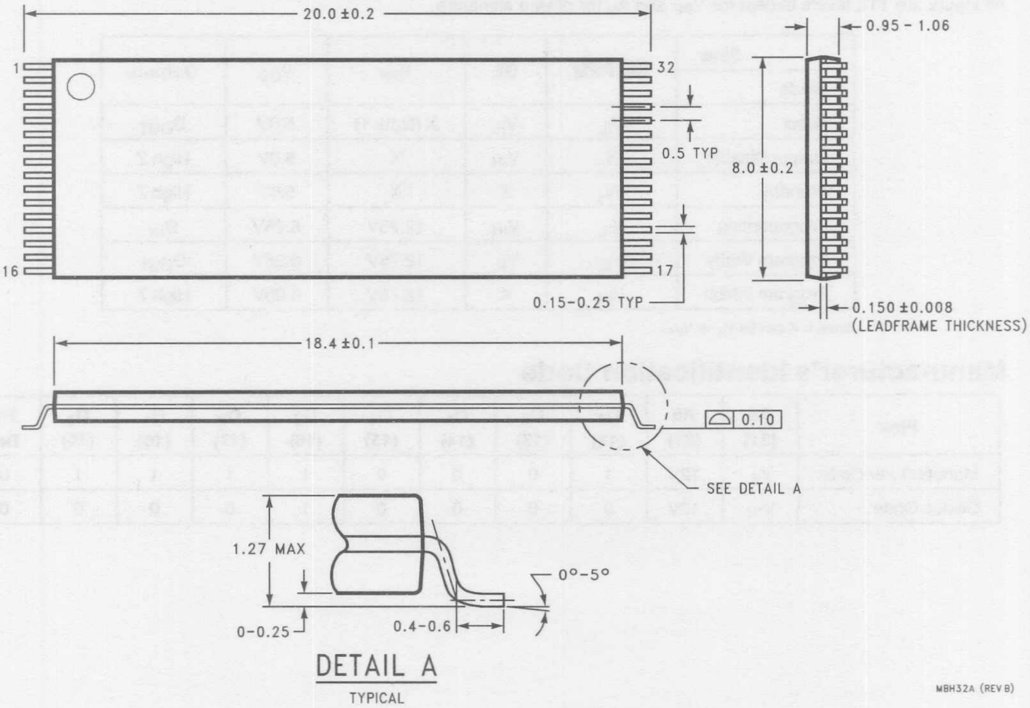
Note 1: X can be V_{IL} or V_{IH}

Manufacturer's Identification Code

Pins	A0 (21)	A9 (31)	O_7 (12)	O_6 (13)	O_5 (14)	O_4 (15)	O_3 (16)	O_2 (17)	O_1 (18)	O_0 (19)	Hex Data
Manufacturer Code	V_{IL}	12V	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	12V	0	0	0	0	1	0	0	0	08

Lit # 112256-002

Physical Dimensions inches (millimeters) (Continued)



32-Lead Thin Small Outline Package
Order Number NM27LV040Txxx
NS Package Number MBH32A

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
2900 Semiconductor Drive
P.O. Box 58090
Santa Clara, CA 95052-8090
Tel: 1(800) 272-9959
TWX: (910) 339-9240

National Semiconductor GmbH
Industriestrasse 10
D-82256 Fürstenfeldbruck
Germany
Tel: (0-81-41) 103-0
Telex: 527649
Fax: (0-81-41) 10-35-06

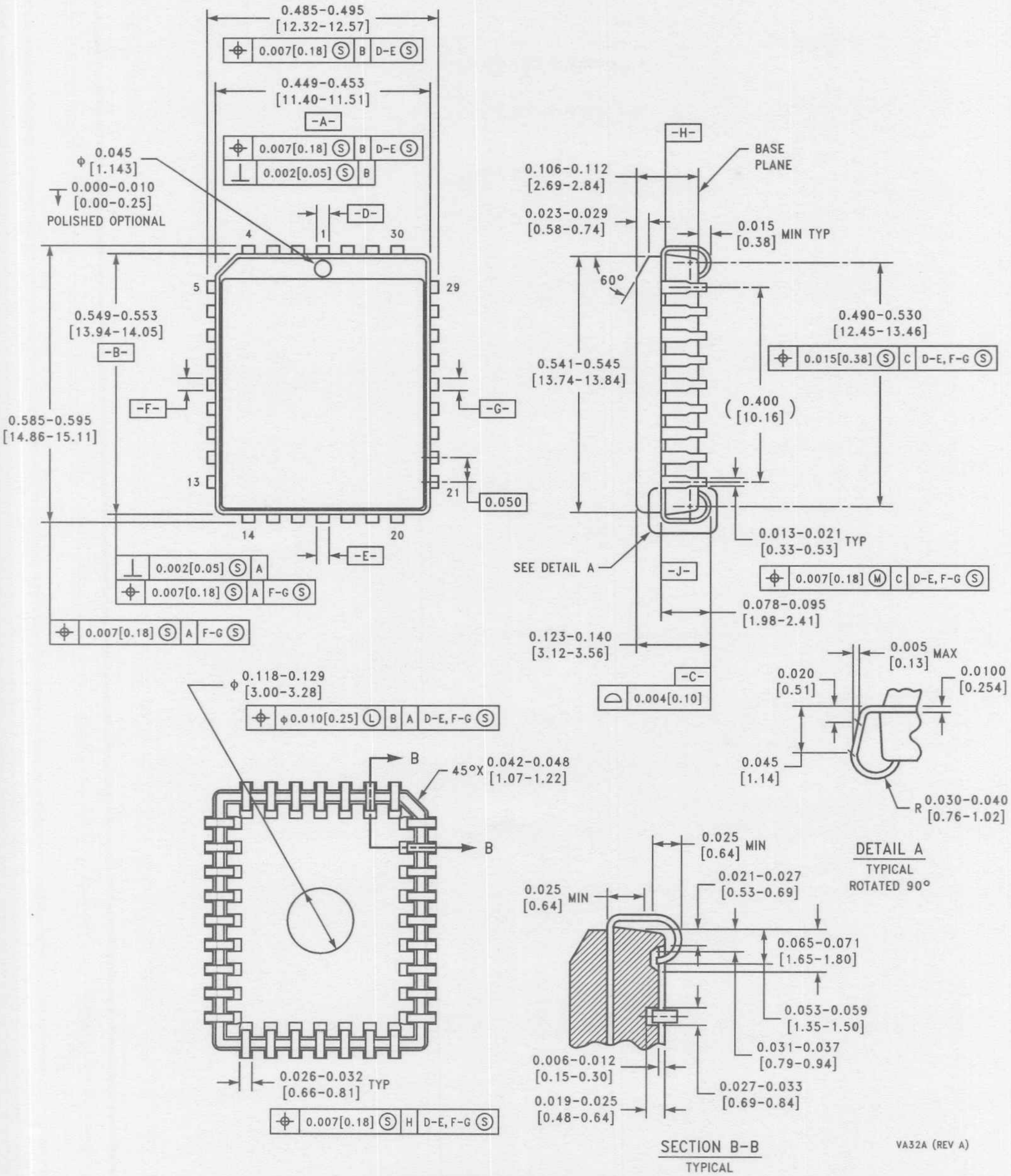
National Semiconductor Japan Ltd.
Sumitomo Chemical Engineering Center
Bldg. 7F
1-7-1, Nakase, Mihama-Ku
Chiba-City,
Ciba Prefecture 261
Tel: (043) 299-2300
Fax: (043) 299-2500

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 737-1600
Telex: 51292 NSHKL
Fax: (852) 736-9960

National Semiconductores Do Brazil Ltda.
Rue Deputado Lacorda Franco 120-3A
Sao Paulo-SP
Brazil 05418-000
Tel: (55-11) 212-5066
Telex: 391-1131931 NSBR BR
Fax: (55-11) 212-1181

National Semiconductor (Australia) Pty, Ltd.
16 Business Park Dr.
Notting Hill, VIC 3168
Australia
Tel: (3) 558-9999
Fax: (3) 558-9998

Physical Dimensions inches (millimeters)



32-Lead PLCC Package (V)
Order Number NM27LV040Vxxx
NS Package Number VA32A